Short Papers

A Large-Signal HSPICE Model for the Heterojunction Bipolar Transistor

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Abstract—**The emergence of the heterojunction bipolar transistor (HBT) from digital integrated circuit designs to analog/microwave MMIC applications has led to the need for accurate nonlinear models at microwave frequencies. The ability to predict performances of RF circuits such as mixers, voltage-controlled oscillators, and amplifiers is very important to the first-pass success of MMIC chip designs. The development of an accurate HSPICE model for the $3\times 10\ \mu m^2$ HBT allows the simulation of nonlinear measurements such as gain at the 1 dB compression point ($P_{1\ dB}$) and third-order intercept point (IP3) for circuit designs utilizing this emerging technology.**

I. Introduction

The emergence of GaAs heterojunction bipolar technology into the field of microwave circuit design applications has given rise to a need for more accurate device models at microwave frequencies, especially if these designs are to be implemented in monolithic form with any chance of first-pass success. Nonlinear models permit simulations of such key circuit performance parameters as 1 dB compression ($P_{1\ dB}$) and third-order intercept points (IP3), vital specifications for almost any MMIC chip in today's systems applications. The development of a HSPICE model for the HBT is an important tool for these nonlinear simulations. This paper describes the development of an HBT HSPICE model and its application to MMIC chip designs.

II. HBT Fabrication Technology

The HBT devices which were characterized were fabricated with an analog/digital IC process that facilitates high performance and high yield. Fig. 1 illustrates the molecular-beam epitaxy (MBE) single heterostructure which is used to grow the npn HBT emitter-up on semi-insulating (undoped LEC) GaAs/AlGaAs. The growth structure focuses on maximizing current gain and high-frequency performance. Key features include linearly graded aluminum at the emitter–base interface to suppress the heterojunction barrier spike, highly doped thick Be p-base to minimize base resistance, and lightly doped thick collector layer to minimize collector capacitance and to increase the collector–base breakdown voltage [1], [2]. No material enhancements such as built-in drift fields or velocity overshoot structures were implemented, and the self-aligned mesa IC process (11 mask levels) shown in Fig. 2 is used to integrate key device components including transistors, Schottky diodes, laser trimmable thin-film resistors, and metal–insulator–metal (MIM) capacitors [3]. The active device layers are accessed by a combination of selective and nonselective wet chemical etches. Ohmic contacts are formed by AuBe/Pd/Au and AuGe/Ni/Ti/Au for p-type and n-type ohmic contacts, respectively. Plasma-enhanced CVD silicon nitride is used to passivate the GaAs surface and serves as a dielectric insulator for MIM capacitors and double-level metal interconnection (Ti/Pt/Au and Ti/Au). Ti/Pt/Au is used as the first interconnect metal and also serves as the Schottky barrier metal for diodes [3].

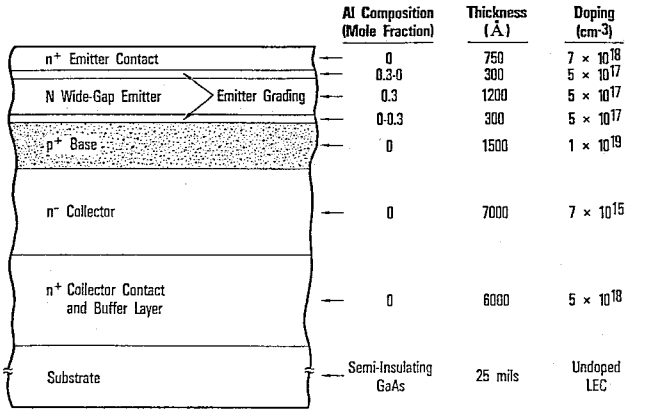

Fig. 1. Molecular-beam epitaxy GaAs/AlGaAs HBT growth structure.

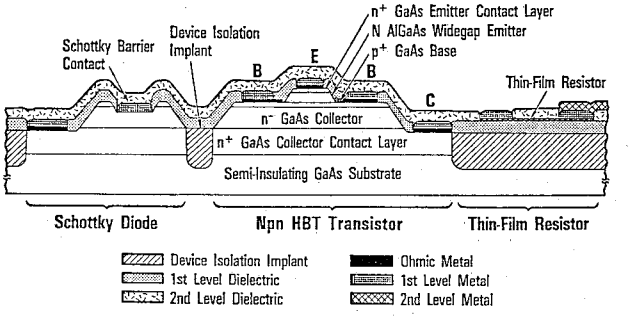

Fig. 2. Integrated circuit fabrication structure cross section with HBT transistor, Schottky diode, and thin-film resistor.

TABLE I
MEASURED AC AND DC HBT PARAMETERS

dc Parameters:	
Transportation saturation current	I_S
Forward current emission coefficient	N_F
Base–emitter leakage saturation current	I_{SE}
Base–emitter leakage emission coefficient	N_E
Base–collector leakage saturation coefficient	I_{SC}
Base–collector leakage emission coefficient	N_C
Forward current gain	β_F
Reverse current gain	β_R
Forward Early voltage	V_{AF}
Reverse Early voltage	V_{AR}
Emitter contact resistance	R_{EE}
Collector contact resistance	R_{BB}
Base resistance (contact and intrinsic)	ΣR_B's
ac Parameters:	
S parameters from 1 to 18 GHz	$S_{11}, S_{21}, S_{12}, S_{22}$
Bias conditions: $V_{CE}=1$–5 V; $I_C=1$–5 mA	

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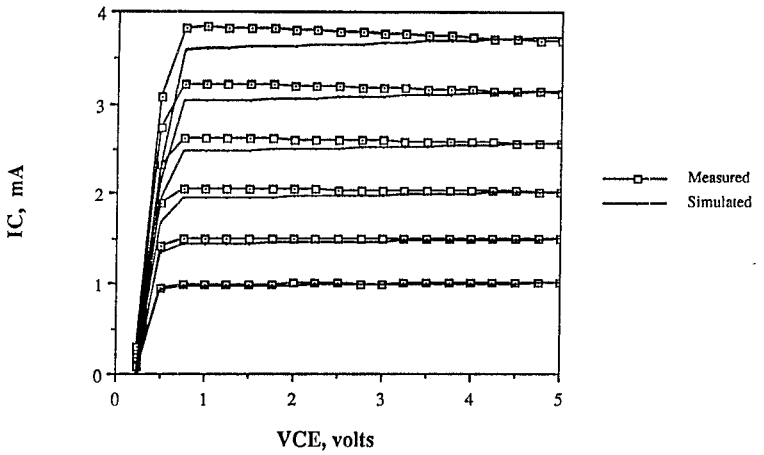


Fig 3. Comparison of measured and simulated IV curves

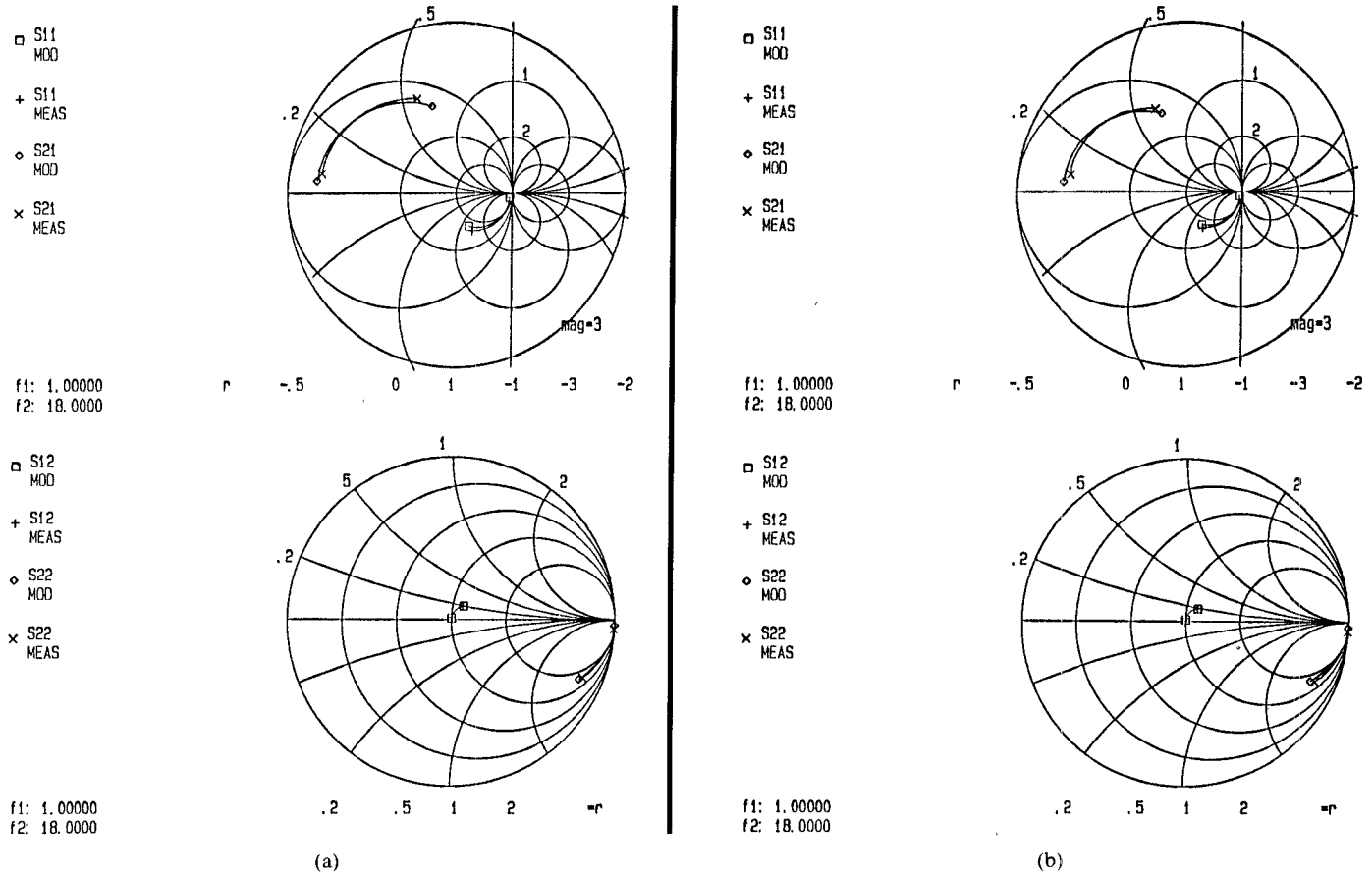


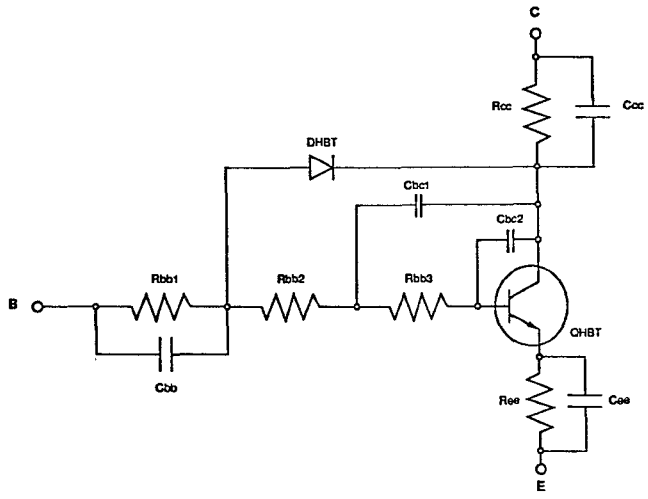
Fig. 4. Comparison of measured and simulated S parameters (1–18 GHz) over various bias conditions. MOD = simulated results; MEAS = measured results (a) $V_{CE} = 3$ V; $I_C = 2.6$ mA. (b) $V_{CE} = 3$ V; $I_C = 4.4$ mA.

The standard HBT device uses a $3 \times 10\ \mu m^2$ single emitter–base junction. These devices, which are able to attain high dc current gains ($\beta = 100$ at 1 mA of collector current) and excellent device-matching characteristics (V_{be} matching ≈ 1–2 mV), are also capable of f_T's in the 25–50 GHz region. The Early voltage ($V_A \approx 150$ V) is also a factor of 10 higher than silicon bipolars of comparable microwave performance, with devices capable of maximum available gains of approximately 10 dB at the lower *Ku*-band frequencies. These performance characteristics make the HBT an excellent candidate not only for digital but also for microwave circuit design applications.

III. HBT Model Development

A. Device Characterization

Extensive measurements of the HBT's various ac and dc parametric values were taken in order to build up statistical mean and variance data pertaining to this particular device type ($3 \times 10\ \mu m^2$ single-emitter device). The dc (IV; current–voltage) measurements were used to determine the forward and reverse saturation currents, Early voltages, and β current gains. Direct measurements of such parameters as the base, emitter, and collector contact resistances, as well as base sheet resistance, were also



SPICE Parameters

	Bipolar Junction Transistor, QHBT		Diode, DHBT
Rbb1 = 9 Ohms			
Rbb2 = 12 Ohms			
Rbb3 = 9 Ohms	IS = 8E-24 amps	RE = 0.0 Ohms	IS = 1.0E-24 amps
Rcc = 4 Ohms	NF = 1.179	BF = 169	RS = 0.7 Ohms
Ree = 3 Ohms	ISE = 30E-21 amps	BR = 0.1	CJO = 13 fF
Cbc1 = 3 fF	NE = 1.6	VJE = 1.7 volts	N = 1.7
Cbc2 = 3 fF	RB = 34 Ohms	MJE = 0.5	M = 0.5
Cbb = 18 fF	RC = 6 Ohms	CJE = 17 fF	PB = 1.7
Ccc = 37 fF	VJC = 1.21 volts	TF = 4 psec	
Cee = 114 fF	MJC = 0.5 volts	VAF = 150 volts	

Fig. 5. HSPICE model for the $3\times10\ \mu m^2$ single-emitter HBT.

taken via measurements of special test structures (Kelvin cross bridge measurements). Measurements of the device S parameters over a 1 to 18 GHz frequency range were obtained at various bias points ($V_{CE}=1$–5 V, $I_C=1$–5 mA) in order to determine the bias-dependent relationships of the device parameters. Table I lists the ac and dc parameter measurements obtained.

B. HBT Nonlinear HSPICE Model

HSPICE was selected as the simulation tool due to its versatility in small- and large-signal circuit simulation capabilities and because of its capability to perform optimization of device model parameters to fit measurement data. Once the measured results were recorded, the first approximation at the dc parameters of the device was determined. Using the measured IV data as the goal, the device dc model parameters (I_S, I_{SE}, N_F, N_E, β_F, β_R, R_E, R_C, and R_B) were optimized for the best match to the measured dc performance (see Fig. 3). All ac parameters such as the device intrinsic and parasitic capacitances were held constant at preliminary values. Upon convergence, the dc parameters were fixed and the ac model parameters (PTF excess phase factor, τ_F, C_{BC}, C_{JE}, C_{JO}, C_{BB}, C_{CC}, and C_{EE}) were optimized for best fit to the measured S parameters at several bias points (see Fig. 4) and very good correlation was achieved. The resulting HSPICE model is shown in Fig. 5.

C. Comparison with Measured Results

Measurements of the HBT's 1 dB compression point and IP3 performance were taken with the device in a test fixture and its input and output matched for optimal gain at 12.5 GHz. Under bias conditions of $V_{CE}=3$ V and $I_C=4$ mA, the 1 dB compression point was found to occur at approximately +4.5 dBm while the device's IP3 was determined to be +20.5 dBm. Comparing these measured results to the large-signal HBT model simulation predictions (see Fig. 6) of a 1 dB compression point of +3.5 dBm

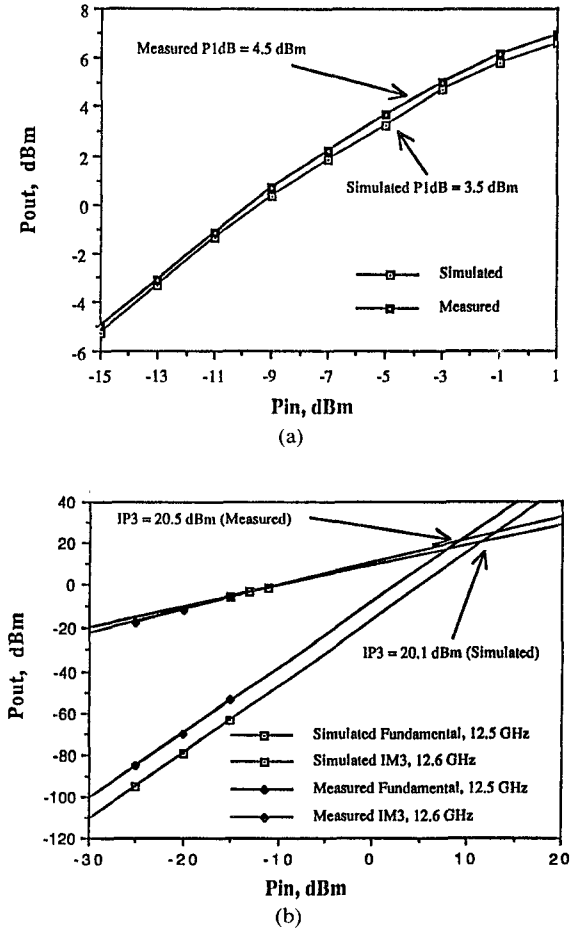


Fig. 6. Comparison of simulated and measured results. $V_{CE}=3$ V; $I_C=4$ mA. (a) P_{in}/P_{out} (1 dB compression point). Frequency = 12.5 GHz. (b) IP3 (third-order intercept point). Two tone input frequencies at 12.4 and 12.5 GHz.

and an IP3 of +20.1 dBm indicates that the derived HSPICE model is an accurate representation of the $3\times10\ \mu m^2$ single-emitter HBT. Note that the IP3 value is approximately 16 dBm greater than the 1 dB compression point, whereas typical MESFET and silicon bipolar devices have IP3 values ranging between approximately 10 to 13 dBm greater than the 1 dB compression point. This result indicates that the HBT is an excellent candidate for circuit applications where high linearity is required.

IV. Conclusion

In this paper, we have presented an accurate nonlinear model of the $3\times10\ \mu m^2$ single-emitter HBT device. The comparison with experimental data on 1 dB compression point and IP3 confirms the validity of the model. This model is now being extensively used in HBT circuit designs.

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References

[1] M. E. Kim, J. B. Camou, A. K. Oki, K. S. Stolt, and V. M. Mulvey, "GaAs/$Al_{0.3}Ga_{0.7}As$ heterojunction bipolar transistors and integrated circuits with high current gain for small device geometries," *1986 GaAs IC Symp. Tech. Dig.*, pp. 163–166.

[2] A. K. Oki *et al.*, "High performance GaAs/AlGaAs heterojunction bipolar transistor 4-bit and 2-bit A/D converters and 8-bit D/A converter," in *1987 GaAs IC Symp. Tech. Dig.*, pp. 137–140
[3] G M. Gorman, J. B. Camou, A. K. Oki, B. K. Oyama, and M E. Kim, "High performance sample-and-hold implemented with GaAs/AlGaAs heterojunction bipolar transistor technology," in *1987 IEDM Tech. Dig.*, pp 623–626.

Computer-Aided Design of Hybrid and Monolithic Broad-Band Amplifiers for Optoelectronic Receivers

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Abstract — **In very high data rate fiber-optic systems, it is necessary to have an ultra-wide-band, high-gain, low-noise amplifier after the front end. This paper shows how powerful analytical techniques, such as the real frequency technique, may be applied to the design of a 4 MHz–7 GHz amplifier. A two-stage monolithic amplifier designed according to the theory gives 17 dB gain; a three-stage hybrid amplifier exhibits 16 dB gain across the same frequency band.**

I. Introduction

The real frequency technique [1], [2] has until now been applied to broad-band amplifier design covering two to three octaves. In very high data rate fiber-optic systems, it is necessary to have bandwidth spanning typically three decades. Thus an optical receiver for a 4.8 Gbit/s direct detection system (NRZ code) needs an amplifier with a 6 MHz–6 GHz bandwidth (Fig. 1). Until now, multidecade amplifier design has been largely based upon empirical principles [3]. In this paper, we apply the real frequency technique to the design of a 4 MHz to 7 GHz, 50 Ω amplifier. This method utilizes only the measured scattering parameters of the FET devices. Neither *a priori* knowledge of an equalizer topology nor an analytic form of the system transfer function is assumed. The optimization process of the design procedure is performed simultaneously on the transducer power gain and the *VSWR* using a modified least-squares Marquardt routine which is described by More [4]. Two versions of the amplifier were studied: a two-stage monolithic amplifier realized using the Plessey III–V foundry, and a three-stage hybrid amplifier. The gain, noise figure, and pulse response of each amplifier are presented.

II. Circuit Topology

At low frequencies microwave GaAs MESFET's are unstable and are virtually impossible to match over large bandwidths. This is mainly due to the high input reflection coefficient and the high gain of the device. It is thus necessary to use either lossy matching or *RL* feedback to reduce terminal impedances and stabilize the transistor [3]. A solution integrating both methods has been adopted in our case. The GaAs MESFET is thus embedded in a network including a parallel feedback loop, a drain series inductance, and a gate shunt resistance to form an elementary module termed the transistor feedback block (TFB,

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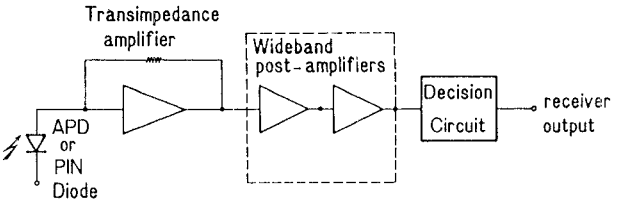

Fig. 1. Fiber-optic system receiver front end.

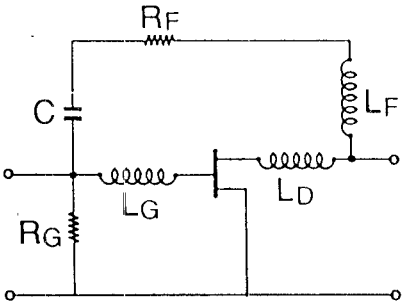

Fig 2 Transistor feedback block (TFB) design.

Fig. 2). This block is designed using the following approach [3]:

- First we choose a value of the feedback resistor, R_F, which gives us a perfect match: $R_F = g_m Z_0^2$.
- But in general $R_F > g_m Z_0^2$; then R_F is made selective by L_F to reduce feedback at higher frequencies. L_D is introduced to compensate for transistor C_{DS}. L_G allows input match and high frequency gain.
- A decoupling capacitor C is introduced into the feedback loop. $C = 50$ pF is a compromise between a high value required to maintain feedback to the lowest frequency possible and minimizing parasitic effects. A damping resistor R_G is introduced to prevent low-frequency oscillations.
- In order to further extend the bandwidth and to improve the gain and *VSWR* performance of the amplifier, the multistage synthesis method outlined in the following section is applied, with the TFB replacing the GaAs MESFET (including also interstage capacitor and bias network) as the active element. Finally the entire TFB is optimized for maximum gain flatness across the widest frequency band.

III. Synthesis Method

The real frequency technique, introduced by Carlin [1], is an optimum approach to broad-band matching. This technique has been extended to double matching and multistage microwave amplifiers [2]. In this section we show how the real frequency technique for multistage matching microwave TFB can be extended to optimize gain and *VSWR*. The optimization is based on a modified least-squares Marquardt routine.

A. The Simplified Real Frequency Technique [2]

In the case of the double matching problem, it has been shown [5] that the scattering parameters of an equalizer, E, can be completely determined from the numerator polynomial $h(p)$ of the input reflection $e_{11}(p)$. E is assumed to be a ladder network; thus the scattering parameters are given as (Belevitch representa-

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